U.S. Application No.	International Application No. PCT/BE98/00139	Attorney Docket No. IMEC169.001APC

Date: May 12, 1999 Page 1

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 USC 371

International Application No.:PCT/BE98/00139
International Filing Date: September 22, 1998
Priority Date Claimed:
Title of Invention: DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR
Applicant(s) for DO/EO/US: Bart Dierickx and Spyros Kavadias

Assistant Commissioner for Patents
Box PCT
Washington D.C. 20231-9998

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. (X) This is a **FIRST** submission of items concerning a filing under 35 USC 371.

2. () This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 USC 371.

3. (X) This express request to begin national examination procedures (35 USC 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 USC 371(b) and PCT Articles 22 and 39(1).

4. () A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. (X) A copy of the International Application as filed (35 USC 371(c)(2))

    a) (X) is transmitted herewith (required only if not transmitted by the International Bureau).
    b) () has been transmitted by the International Bureau.
    c) () is not required, as the application was filed in the United States Receiving Office (RO/US).

6. () A translation of the International Application into English (35 USC 371(c)(2)).

7. (X) Amendments to the claims of the International Application under PCT Article 19 (35 USC 371(c)(3))

    a) () are transmitted herewith (required only if not transmitted by the International Bureau).
    b) () have been transmitted by the International Bureau.
    c) () have not been made; however, the time limit for making such amendments has NOT expired.
    d) (X) have not been made and will not be made.

8. () A translation of the amendments to the claims under PCT Article 19 (35 USC 371(c)(3)).

9. () An oath or declaration of the inventor(s) (35 USC 371(c)(4)).

10. () A copy of the International Preliminary Examination Report with any annexes thereto, such as any amendments made under PCT Article 34.

U.S. Application No.   International Application No.   Attorney Docket No.

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11.   ( )   A translation of the annexes, such as any amendments made under PCT Article 34, to the International Preliminary Examination Report under PCT Article 36 (35 USC 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

12.   ( )   An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

13.   ( )   An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

14.   (X)   A FIRST preliminary amendment.
         ( )   A SECOND or SUBSEQUENT preliminary amendment.

15.   ( )   A substitute specification.

16.   ( )   A power of attorney and/or address letter.

17.   (X)   International Application as published.

18.   ( )   Small Entity Statement.

19.   ( )   PCT Form PCT/IPEA/402.

20.   (X)   PCT Form PCT/IB/308.

21.   (X)   PCT request form.

22.   (X)   International Search Report Form PCT/ISA/210

23.   (X)   Notification of the Recording of a Change.

24.   (X)   A return prepaid postcard.

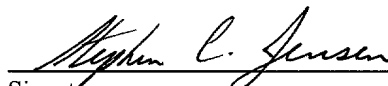25.   (X)   The following fees are submitted:

				FEES
	BASIC FEE			$840

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	
Total Claims	7 - 20 =	0 ×	$18	$0
Independent Claims	2 - 3 =	0 ×	$78	$0
Multiple dependent claims(s) (if applicable)			$260	$0
	TOTAL OF ABOVE CALCULATIONS			$840

Reduction by 1/2 for filing by small entity (if applicable). Verified Small Entity $
statement must also be filed. (NOTE 37 CFR 1.9, 1.27, 1.28)

	TOTAL NATIONAL FEE			$840
	TOTAL FEES ENCLOSED			$840
		amount to be refunded:		$
		amount to be charged:		$

26.   (X)   The fee for later submission of the signed oath or declaration set forth in 37 CFR 1.492(e) will be paid upon submission of the declaration.

27.   (X)   A check in the amount of $840 to cover the above fees is enclosed.

28.   ()   Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40 per property.

29.   (X)   The Commissioner is hereby authorized to charge only those additional fees which may be required to avoid abandonment of the application, or credit any overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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IMEC169.001APC   PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Dierickx et al.	)	Group Art Unit Unknown
			)	
Int'l Appl. No. :		PCT/BE98/00139	)	
			)	
Int'l Filing Date:		September 22, 1998	)	
			)	
For	:	DEVICES AND METHOD FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR	))))	
			)	
Examiner	:	Unknown	)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please delete Claims 5 and 9.

1.   (Amended) An image sensor comprising an array of rows (i) and columns (j) of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element (M_j) and at least a first amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterized in that the sensor further comprises:

a second amplifying element (B_j) on the output of the memory element (M_j),

said common output amplifier (D) having at least two input terminals,

means (S1) for switching the pixel's signal on the common output line (l_j) and the memory element's signal (M_j) to respectively third and second amplifying elements (A_j and B_j) of one column, and

-1-

means (S2) for switching the two output signals of the amplifying elements (A$_j$, B$_j$) of one column to respectively first and second input terminals of said common **[output]** amplifier (D).

3. (Amended) An image sensor comprising an array of rows and columns of pixels (X$_{ij}$), all the pixels of one column of the array being connected to at least one common pixel output line (l$_j$) having at least one memory element (M$_j$) and at least one amplifying element (A$_j$), all these amplifying elements (A$_j$) being connected to a common output amplifier (D), characterized in that before the amplifying element (A$_j$), the common pixel output line (l$_j$) is divided through switches (S4$_j$ and S5$_j$) in at least two parallel circuits, **at least** one circuit having said memory element (M$_j$), **[the two parallel circuits being connected through a switch (S6$_j$) with the same input of said amplifying element (A$_j$)]**.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

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5

DEVICES AND METHODS FOR IMPROVING THE IMAGE QUALITY IN AN IMAGE SENSOR

10

Field of the invention

The present invention relates to solid state imaging devices being manufactured in a CMOS- or MOS- technology.

15   More particularly, the principal object of the present invention is related to methods and devices which are able to improve the image quality in an image sensor.

Another object of the present invention is
20 related to the improvement of the image quality by a method of correcting isolated pixel values present in an image taken by imaging devices.

Background of the invention

25   Solid state image sensors are well known. Virtually all solid-state imaging sensors have as key element a photosensitive element being a photoreceptor, a photo diode, a photo transistor, a CCD gate, or alike. Typically, the signal of such a photosensitive element is a
30 current which is proportional to the amount of electromagnetic radiation (light) falling onto the photosensitive element.

A structure with a photosensitive element included in a circuit having accompanying electronics is

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called a pixel. Such pixel can be arranged in an array of pixels so as to build focal plane arrays of rows and columns.

Commonly such solid state image sensors are
5   implemented in a CCD-technology or in a CMOS- or MOS-technology. Solid state image sensors find a widespread use in devices such as camera systems. In this application a matrix of pixels comprising light sensitive elements constitutes an image sensor, which is mounted in the camera
10 system. The signal of said matrix is measured and multiplexed to a so-called video-signal.

Of the image sensors implemented in a CMOS- or MOS-technology, CMOS or MOS image sensors with passive pixels and CMOS or MOS image sensors with active pixels are
15 distinguished. An active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element. Passive pixels do not have said means and require a charge sensitive amplifier that is not integrated in the pixel. For this
20 reason, active pixel image sensors are potentially less sensitive to noise fluctuations than passive pixels. Due to the additional electronics in the active pixel, an active pixel image sensor may be equipped to execute more sophisticated functions, which can be advantageous for the
25 performance of the camera system. Said functions can include filtering, operation at higher speed or operation in more extreme illuminations conditions.

Examples of such imaging sensors are disclosed in EP-A-0739039, in EP-A-0632930 and in
30 US-A-5608204. The imaging devices based on the pixel structures as disclosed in these patent applications however are still subject to deficiencies in the image quality of the devices.

A problem in these CMOS based imaging devices appears because material imperfections and technology variations have as effect that there is a non-uniformity in the response of the pixels in the array. This effect is

5   caused by a non-uniformity or fixed pattern noise (FPN) or by a photoresponse non-uniformity (PRNU). Correction of the non-uniformity needs some type of calibration, e.g. by multiplying or adding/subtracting the pixel's signals with a correction amount that is pixel-dependent.

10   Several methods to cancel FPN are based on techniques that are often called correlated double sampling or offset compensation. The methods in general are based on the following: the signal of the pixel is subtracted from the signal of the same pixels in a reference state (this

15   reference state is typically the reset or dark state). The difference of both signal is free of pixel-related non-uniformity. However, if the differencing circuit is common for a part of the imager (typically, common for one column), a new non-uniformity will originate due to the

20   non-uniformity of the differencing circuits. In a typical APS imager with common column buffers or column amplifiers, the new fixed pattern noise is column dependent, and is visible in the image as a shade of vertical stripes.

A stripe-shaped FPN is much more annoying

25   than a pure statistical FPN. It is seen in experiments that a true random FPN of 5% RMS is barely visible to the human eye, whereas a stripe-shaped FPN remains visible even when the amplitude is below 1% RMS. The reason is that the human eye has a kind of built-in spatial filter that recognises

30   larger structures even when they have low contrast.

Even if in the case that we have no fixed pattern noise, the photoresponse non-uniformity can be different from 0.

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Another problem arises due to processing imperfections, statistics, etc. This means that typically, a finite number of pixels in a pixel array will be defective (hard faults) or yield a signal that deviates

5 visibly from the "exact" pixel value. Such faults appear as white or black (or grey) points in the image. This class of faults in the sequel is called an isolated pixel value.

A known way to cancel these spots is to store a list of them and of their positions in the image in a

10 memory unit in the device. In an image processing step, the isolated pixel value is then replaced by e.g. the average of the surrounding pixels. This method is viable, but has the disadvantage that it requires a memory. Moreover, it cannot handle isolated pixel values that appear

15 intermittently or only in certain cases. A good example, is a so-called dark current pixel. Such pixels will appear white in a dark environment, but will behave normal in a bright environment.

Other ways to cancel isolated pixels faults

20 have been proposed, e.g. the spatial median filter or other types of Kalman filters can be used to remove such isolated faults. Unfortunately, such filters do also remove useful detail from the image. Consider the image of a star covered sky with an image sensor that has some faulty pixels that

25 appear white. The quoted filters are not able to remove the white point due to faults, and leave the white points that are stars untouched.

Aim of the invention

30 The present invention aims to suggest a pixel structure and methods to improve the image quality, more in particular the image non-uniformity of in array of pixels by cancellation of the appearance of column-shaped fixed pattern noise (FPN).

Main characteristics of the present invention

As a first object, the present invention is related to an image sensor comprising an array of rows and columns of pixels, all the pixels of one column of the array being connected to at least one common pixel output line having at least one memory element and at least a first amplifying element, all these amplifying elements being connected to a common output amplifier.

According to one preferred embodiment, the image sensor further comprises :

- a second amplifying element on the output of the memory element,

- said common output amplifier having at least a first and a second input terminals,

- means for switching the pixel's signal on the common output line and the memory element's signal to respectively first and second amplifying elements of one column, and

- means for switching the two output signals of the amplifying elements of one column to respectively first and second input terminals of said common output amplifier.

Preferably, the switching means comprise at least one cross-bar switch.

According to another preferred embodiment, the image sensor further comprises before the amplifying element two parallel circuits being connected through switches to the common pixel output line, at least one circuit having said memory element. Preferably, both circuit have a memory element.

According to another preferred embodiment, said common pixel output line is being connected through switches to said memory element and said amplifying

element, where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element during the second phase of the read-

5   out.

The present invention is also related to a method of reading out an array of rows and columns of pixels in an image sensor as described hereabove according to the first embodiment, comprising the steps of:

10   - amplifying the output signals of essentially each pixel of one column in the first amplifying element thereby obtaining a set of amplified pixel output signals,

- amplifying the reference signals of essentially each pixel of one column in the second amplifying element,

15   thereby obtaining a set of amplified pixel reference signals,

- consecutively, for essentially each pixel of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier and

20   imposing the amplified pixel reference signal to a second or a first terminal of said common output amplifier, while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said

25   column, said reference signal being imposed to the other terminal of said common output amplifier.

A voltage can be imposed to a node. In this case, it means e.g. that the node is connected to a voltage source. The voltage source should be higher than the node,

30   i.e. it should have a lower impedance.

According to another preferred embodiment, the present invention is related to a method of reading out an array of rows and columns of pixels in an image sensor

as described hereabove in the second embodiment of the present invention, comprising the steps of :

- sampling the signal in a first phase and storing it in a memory element,

5 - sampling the signal in a second phase and possibly storing it in another memory element,

- subtracting said first signal from said second signal in a unique output circuit.

According to another preferred embodiment, 10 the present invention is related to a method of reading out an array of rows and columns of pixels in an image sensor as described in the third embodiment of the present invention, comprising the steps of :

- during a first phase, calibrating the output of the 15 amplifying element to a predetermined value,

- storing said value in a memory element during the application of a first signal of said pixel on the line,

- during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal 20 proportional to the difference between first and second signals.

Another aspect of the present invention is related to a method of replacing an isolated pixel value in the image of an image sensor, being an array of pixels, and 25 wherein at least one current source is connected to the pixels, the method comprising the step of :

- limiting said isolated pixel value between or to an upper and/or a lower bound that is derived from the values of pixels in the immediate neighbourhood of the 30 said isolated pixel value.

Preferably, said upper and/or lower bounds are found by extrapolating the immediate neighbourhood pixel values towards a value that corresponds to the

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position of said individual pixel in relation to the immediate neighbourhood pixels.

Said upper and/or lower bounds are found by extrapolating the values of a neighbour (V_1N) of the pixel having said isolated pixel value and of the neighbour thereafter (V_2N), the replacing pixel value being calculated as $V_1N+n*(V_1N-V_2N)$, n being a real number.

The neighbourhood and the neighbourhood thereafter are on the same row of said array. Preferably, the upper bound is the maximum of a set of values, said set being determined as the pixel values (a,b,c,d,e) of pixels on the same row of said array as said isolated pixel, said upper bound being calculated as

cmax = F(a,b,c,d), or cmax G(E(a,b), E(e,d), E(b), E(d))

where F is a non-linear or linear function, G is a non-linear GE or linear function, E is an extrapolating function, wherein cmax= MAX(2b-a,2d-e,b,d)

together with

cmin= MIN(2b-a,2d-e,b,d)

with MAX () yielding the maximum, respectively the minimum of the arguments, the corrected c-value being obtained as

c=MIN(MAX(c,cmin),cmax).

25   **Brief description of the drawings**

Figure 1a   represents a particular implementation of a column FPN cancellation method and the corresponding image sensor structure therefor.

30   **Figure 1b**   represents an embodiment of a cross-bar switch used in the structure represented in Fig. 1a.

Figure 2   describes another particular implementation
                of a column FPN cancellation method and the
                corresponding image sensor structure
                therefor.

5 Figure 3   describes a particular embodiment of an
                output block being used in the structure as
                represented in Fig. 2.

   Figure 4   represents the switching diagram for the
                read-out signal applied to the several
10   switches in the structure as represented in
                Fig. 2.

   Figures 5   represent another particular implementation
                of a column FPN cancellation method and the
                corresponding image sensor structure
15   therefor, wherein Fig. 5a represents more
                particularly one column in an array of pixels
                being connected to two different structures
                represented in details in Fig. 5b and 5c
                during a first phase and a second phase.

20 Figure 6   represents the specific topology used for the
                structure represented in Fig. 5b and 5c.

   Figure 7   represents the switching diagram for the
                read-out sequence to the several switches
                used in the structure represented in Fig. 6.

25 Figures 8a and 8b represent a method of correcting
                isolated white pixel values being present in
                an image composed by an array of pixels.

Brief description of preferred embodiments of the present
30 invention

                As a first object of the present invention, a
   first structure of an APS image sensor is represented in
   Fig. 1. References (X_{1j}), (X_{2j}) and (X_{3j}) are three pixels

of a column of an image sensor. The pixel's signal on a
common output line (l_j) is represented in particular by the
column bus "K" in the present case and is fed to the
optional buffer amplifier A_j, and/or stored on a memory

5 element (capacitor C + switch S3), and fed to amplifier B_j.
By the relative timing of the addressed pixel's reset pulse
and the control of the switch S3, one can make that the
pixel's signal and its reference level are available on
amplifiers A_j, reps. B_j. The fact that the signal passes

10 through the column amplifiers A_j and B_j, is a source of
offset non-uniformity, which is column related and causes a
vertical stripe-shaped FPN. More specifically, each column
will feature an average "OV" offset voltage referred to the
average of the other columns.

15   Switches (S1) and (S2) are crossbar switches.
Suppose that they are in the forward direction either in
crossed directions. Both switches S1 and S2 operate
synchronously. In both cases, the signal on the capacitor C
goes to the input of the output amplifier, and the signal

20 on K goes to the + input of the output amplifier. Yet, the
"OV" of the column will be positive in the one case and
negative in the other case. Since the switches (S1)/(S2)
are modulated, e.g. essentially turned direction at each
new row (i = 1, 2, 3) of the image, the average offset of a

25 column will be zero. For each individual pixel of a column,
there will be indeed remain an offset which is + or − OV
but this is a very small feature, and is not recognised by
the eye as a stripe.

            Another embodiment of the present invention

30 is to suggest a read-out scheme for image sensors that
suppresses the effects of non-uniformities caused by
variations in pixels as well as variations in the output
amplifiers. This read-out scheme can be used in sensors

that provide the output signal in terms of a difference. For example, in a sensor with integrating pixels, this difference is the voltage between the output when the pixel is on reset state and the output voltage after integration
5   time.

Namely the method suggests to subtract the signal when a pixel is reset from the signal after the integration time, in order to have a signal which is free from pixel variations. In order to avoid the introduction
10   of the non-uniform column amplifiers effects, the signal of the reset state as well as the signal after integration are sampled and held by the column read-out circuit. Finally, the subtraction is being carried out by a unique subcircuit at the sensor's output (D). This is detailed in Fig. 2.

15   For every row of pixels the read-out process is, of course, identical. Let us assume that the ith row is selected. When pixels are reset, the switches controlled by the signal $\Phi 1$, are closed, thus the reset-level output of every pixel on the ith row, namely x_{ij}^{r}, is stored on the
20   corresponding memory element M_{rj} (which is in the present case a capacitor).

Then, the switches $S4_j$ controlled by $\Phi 1$ are opened and pixels start integrating the charge carriers produced by the impinging light. After the lapse of the
25   integration time, the switches $S5_j$ controlled by $\Phi 2$ are closed, thus storing the values of the pixel output to the memory element M_{sj} (also a capacitor). This value, for the pixel with coordinates ij is denoted as x_{ij}^{s}.

After the sample and hold phase for the two
30   voltages, x_{ij}^{r} and x_{ij}^{s}, for the first column and by proceeding from the first column to the last, the

appropriate column read-out circuit is connected with the output.

When the ith column has been selected, the signal Φ3 drives the switch S6ⱼ to led the signal x_{ij}^r to

5   the output modified according to the action of the column amplifier, so as a signal

$$y_{ij}^s = A_j\, x_{ij}^s + B_j \qquad (1)$$

is led to block D (common output amplifier).

The block D is an easily realisable circuit

10 with an output

$$z(n) = [y(n) - y(n-1)] \qquad (2)$$

where y(n) denotes the input as instant n.

A preferred embodiment of such output block (D) is described in details in Fig. 3. Therefore, the

15 output signal will be free from variations in the characteristics of pixels and the column amplifiers.

$$y_{ij}^r - y_{ij}^s = A_j\left(x_{ij}^r - x_{ij}^s \right) \qquad (3)$$

where Aⱼ is easily reproducible, by example by using source followers as the local final phase of the column circuits

20 (when Aⱼ = 2, Bⱼ = -V_{thj}).

Fig. 4 shows a switching diagram for the above-mentioned read-out circuit wherein Φ3 is controlling S4ⱼ, Φ4 is controlling the switch S5ⱼ and Φ5 is controlling the switch S6ⱼ.

25   According to another embodiment of the present invention, an attempt to overcome the problem of offset introduced by the column in a image sensor consisting of pixels is described in Figs. 5 & 6, which can be used with pixels that are read-out twice in every

30 access. For example, in integrating pixels, one read

operation is being performed when the pixel is set on the reset phase (first phase) and the second read-out moment is after a certain integration time (second phase), the first phase is defined by a period wherein the read-out signal of

5   the pixel is according a first state while the second phase is defined by a period such as an integration period where the read-out signal of the pixel is in another state.

In the first phase, when pixel output is V_1, the capacitor C stores a charge :

10   $Q = C(V_{ac}-V_{out}) = C(V_{ac}-V_1+V_{th})$ (4)

where V_{th} is the threshold voltage of μ.

During second phase, when pixel output is V_2, the capacitor stores again charge Q which now can be expressed as :

15   $Q = C(V_{g\mu}-V_2)$ (5)

where $V_{g\mu}$ is the gate voltage of μ.

From (4) and (5), we obtain :

$V_{g\mu} = V_2-V_1+V_{ac}+V_{th}$ (6)

Therefore :

20   $V_{out} = V_2-V_1+V_{ac}$ (7)

i.e. the output voltage does not depend on the V_{th} (where variations in the V_{th} cause offsets in the signal V_{out}).

The column amplifier can be implemented by using the topology described in details in Fig. 6.

25   Switches S7, S8, S9, S10 and S11 are being controlled by signals $\Phi5$ and $\Phi6$ (when Φi is high, the corresponding switches are closed) as represented in Fig. 7.

According   to   a   preferred   embodiment

30   represented in Fig. 7, S7, S8 and S9 are controlled by $\Phi5$ while S10 and S11 are controlled by $\Phi6$ (when Φi is high, the corresponding switches are closed). This means that $\Phi5$

is describing the situation represented in Fig. 5b while Φ6 is representing the situation represented in Fig. 5c.

According to another aspect, the present invention is able to discriminate between isolated pixel
5 faults and features in the real image. In the case of an image of a star covered sky, it should be noted that the fact that the image projected through a lens is never perfectly sharp. Even with good lenses, a star image is not projected on a single pixel. Always the point like source
10 of the start will be smeared out over a central pixel and a few neighbours. In a 1-dimensional cross section, a star image will look like the image in Fig. 8a, while an isolated pixel fault will look like in Fig. 8b.

In the above simple example, the peak in
15 Fig. 8b should be removed, while the peak in 8a should remain untouched.

The advantage is clear, only device faults are corrected while normal images are left untouched. The operation causes no visible image degradation in faultless
20 parts of the image.

According to this second aspect of the present invention, a method to remove an isolated whiter or darker pixel from the image is suggested. This method consists in limiting the value of every individual pixel
25 between an upper and/or a lower bound that is/are derived from the values of pixels in the intermediate neighbourhood of the said pixel.

Preferably, the upper and/or lower bounds are found by extrapolation of the neighbourhood pixel values
30 towards the position of the said individual pixel. The upper and/or lower bound are/is a combination of one or several such 1-D or 2-D extrapolations done with different

methods, and/or from different sides of the said individual pixel.

Preferably, extrapolation is the linear extrapolation of a neighbour (N1) of the said individual pixel (IP) and the neighbour thereafter (N2). The extrapolated value is calculated as $2*N1-N2$ or more general: $N1 + n*(N1-N2)$ where the parameter n is a real number, typically between 0 and 3.

According to another preferred embodiment, the calculation of the upper bounds is performed by extrapolating values from the two sides of said individual pixels. The advantage is that only the pixels data in 1 line of an image are required, which saves memory and operations and allows straightforward implementation as a pipelined filter. Also such a filter is able to correct a vertical line defect.

In the example of Figs. 8a and 8b, five pixels in a neighbourhood (a 5-pixel "kernel") are taken. The experience is that smaller kernels do not yield good results. Larger kernels may give some improvements compared to the 5-pixel kernel.

CLAIMS

1. An image sensor comprising an array of
rows (i) and columns (j) of pixels (X_{ij}), all the pixels of
one column of the array being connected to at least one
5   common pixel output line (l_j) having at least one memory
element (M_j) and at least a first amplifying element (A_j),
all these amplifying elements (A_j) being connected to a
common output amplifier (D), characterised in that the
sensor further comprises:

10 – a second amplifying element (B_j) on the output of the
        memory element (M_j),

    – said common output amplifier (D) having at least two
        input terminals,

    – means (S1) for switching the pixel's signal on the common
15   output line (l_j) and the memory element's signal (M_j) to
        respectively third and second amplifying elements (A_j and
        B_j) of one column, and

    – means (S2) for switching the two output signals of the
        amplifying elements (A_j, B_j) of one column to
20   respectively first and second input terminals of said
        common output amplifier (D).

2. An image sensor as recited in claim 1,
wherein said switching means comprise at least one cross-
bar switch.

25   3. An image sensor comprising an array of
columns and rows of pixels (X_{ij}), all the pixels of one
column of the array being connected to at least one common
pixel output line (l_j) having at least one memory element
(M_j) and at least one amplifying element (A_j), all these
30 amplifying elements (A_j) being connected to a common output
amplifier (D), characterised in that before the amplifying

element (A_j), the common pixel output line (l_j) is divided through switches $(S4_j$ and $S5_j)$ in two parallel circuits, at least one circuit having said memory element (M_j).

5   4. An image sensor as recited in claim 3, wherein both circuits have a memory element $(Ms_j$ and $Mr_j)$.

5. An image sensor comprising an array of columns and rows of pixels (X_{ij}), all the pixels of one column of the array being connected to at least one common pixel output line (l_j) having at least one memory element

10   (M_j) and at least one amplifying element (A_j), all these amplifying elements (A_j) being connected to a common output amplifier (D), characterised in that said common pixel output line (l_j) is being connected through switches $(S7_j,$ $S8_j$, $S9_j$ and $S10_j$, $S11_j)$ to a memory element (C_j) and an

15   amplifying element (μ_j), where the offset of the amplifying element is stored on the memory element during a first phase of the read-out, and this offset is subtracted from the signal of the amplifying element during the second phase of the read-out.

20   6. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor according to claim 1, comprising the steps of :

   - amplifying the output signals of essentially each pixel of one column in the first amplifying element (A_j)

25   thereby obtaining a set of amplified pixel output signals,

   - amplifying the reference signals of essentially each pixel of one column in the second amplifying element (B_j), thereby obtaining a set of amplified pixel

30   reference signals,

   - consecutively, for essentially each pixel (i = 1, 2, 3)

of said column imposing the amplified pixel output signal to a first or a second terminal of said common output amplifier (D) and imposing the amplified pixel reference signal to a second or a first terminal of said

5   common output amplifier (D), while switching the amplified pixel output signal to respectively said first and said second terminals for essentially each consecutive pixel of said column, said reference signal being imposed to the other terminal of said common

10   output amplifier.

7. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited in claim 3, comprising the steps of :

- sampling the signal in a first phase and storing it in a

15   memory element (M_{ij}),

- sampling the signal in a second phase and possibly storing it in another memory element,

- subtracting said first signal from said second signal in a unique output circuit (D).

20   8. Method as recited in claim 7, wherein said first phase is the reset phase and said second phase is after the integration period.

9. A method of reading out an array of rows and columns of pixels (X_{ij}) of an image sensor as recited

25   in claim 5, comprising the steps of :

- during a first phase, calibrating the output of the amplifying element to a predetermined value,

- storing said value in a memory element during the application of a first signal of said pixel on the line,

30   - during a second phase, applying a second signal of said pixel on the line in order to have on the output a signal proportional to the difference between first and second signals.
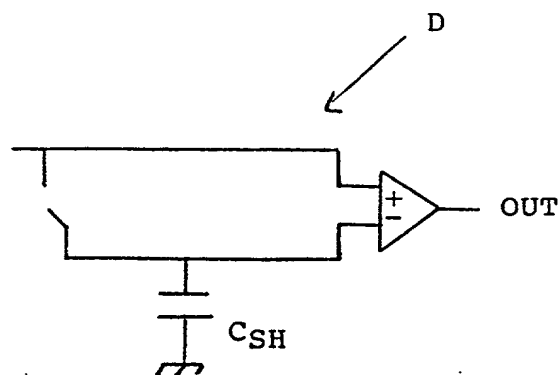
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FIG. 1a

FIG. 1b

FIG. 2

D

OUT

C_{SH}

FIG. 3

row
select

$\phi 3$ S_3

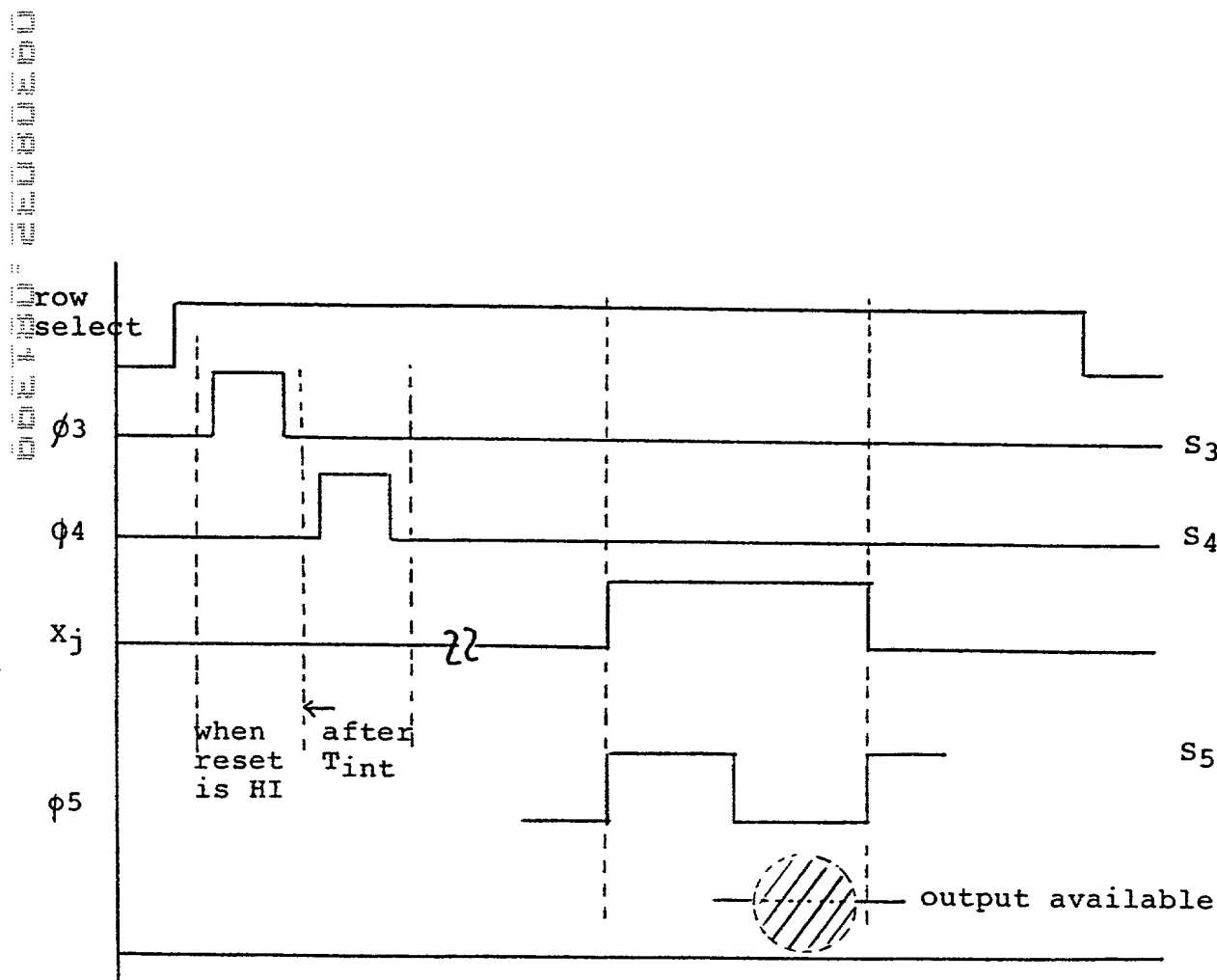$\phi 4$ S_4
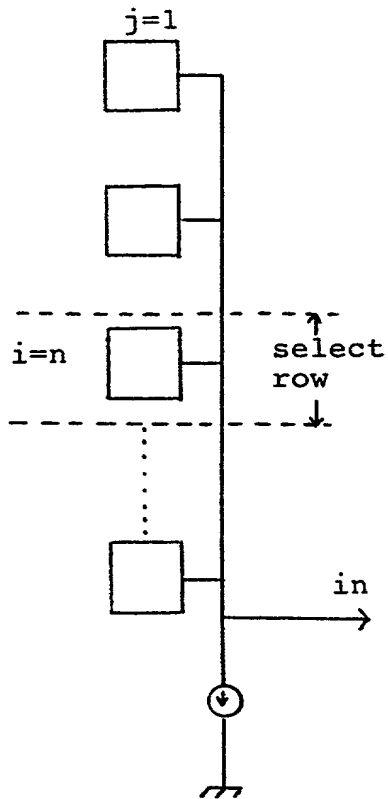
X_j
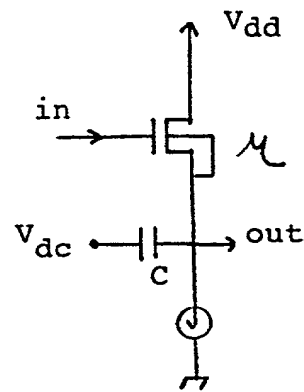
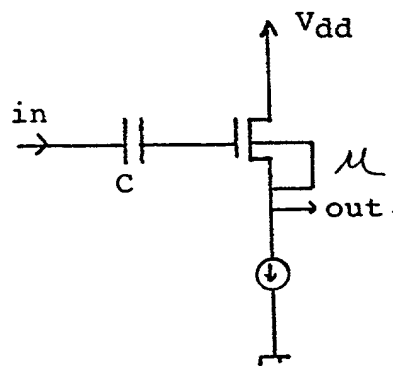when
reset
is HI

after
T_{int}

S_5

$\phi 5$

output available
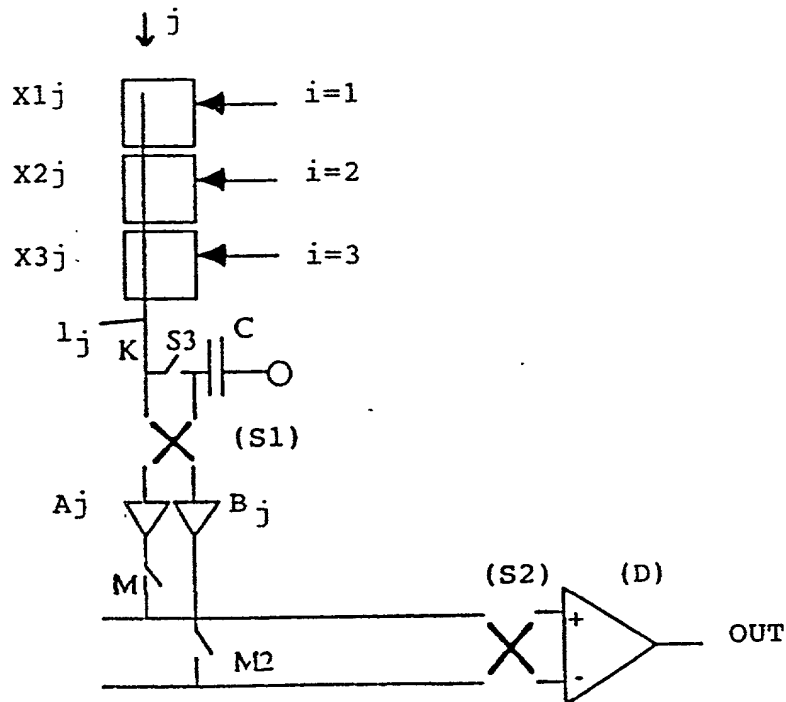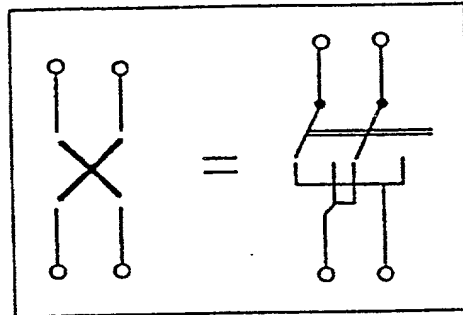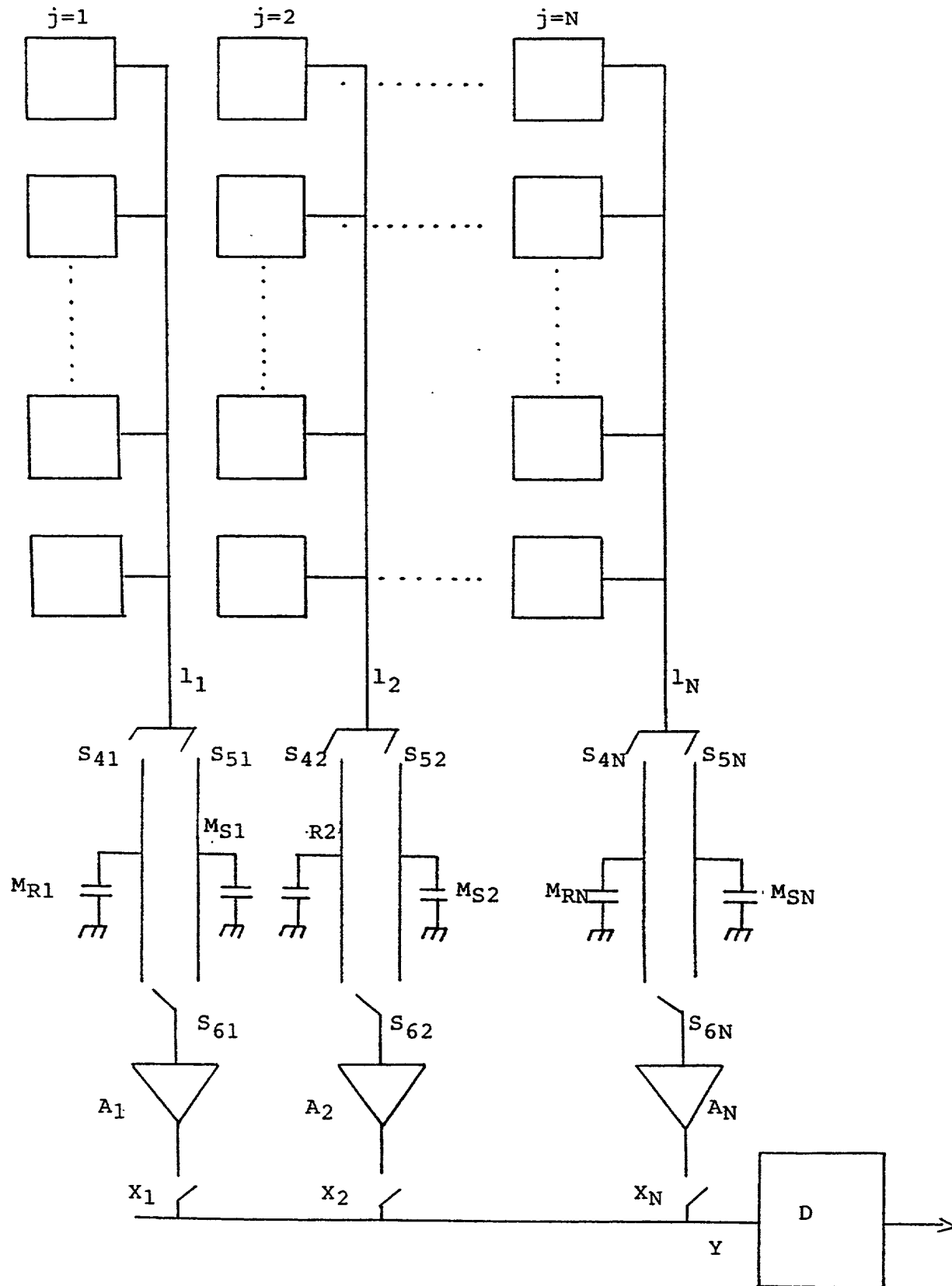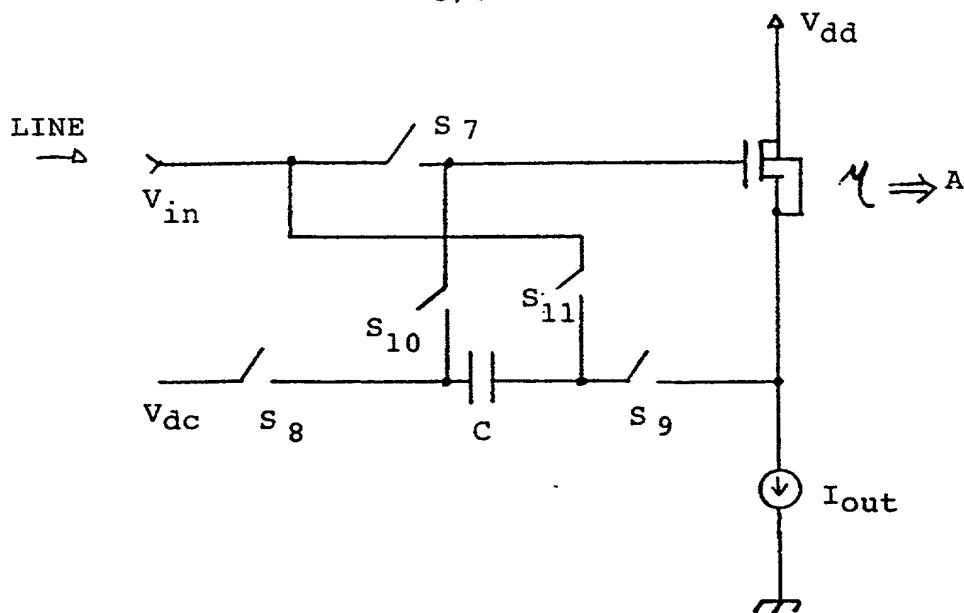
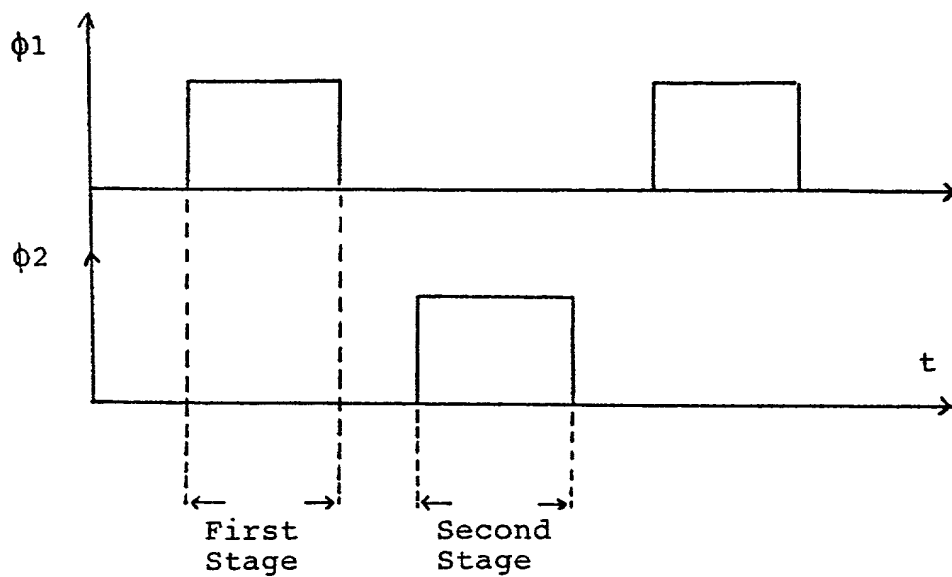FIG. 4

FIG. 5a

FIG. 5b

FIG. 5c
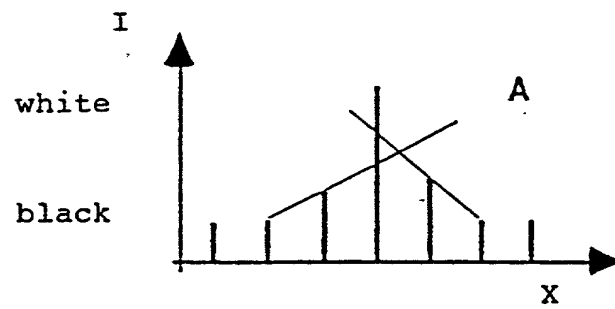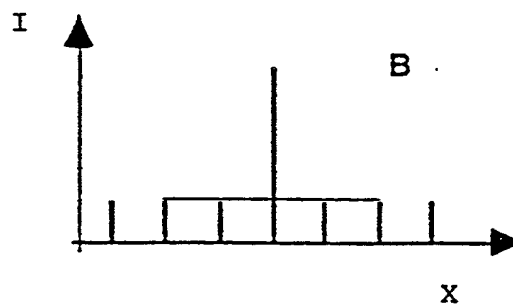
5/6

FIG. 6

FIG. 7

FIG. 8a

FIG. 8b

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Devices and methods for improving the image quality in an image sensor

the specification which was filed on May 12, 1999, Serial No. 09/308,032.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

	Number	Country	Day/Month/Year Filed
1.	EP 978701431	European Patent Office	September 22, 1997
2.	EP 978701704	European Patent Office	October 24, 1997
3.	PCT/BE98/00139	PCT	September 22, 1998

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

	Application Number	Filing Date
1.		
2.		

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

	Application Number	Filing Date	Status: patented, pending, abandoned
1.			
2.			

-1-

Application No. 09/308,032
Filed: May 12, 1999

I hereby appoint the following attorneys and agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:
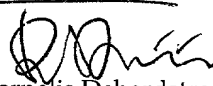
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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